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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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32074	7590	01/30/2006	EXAMINER	
INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			CAMPOS, YAIMA	
			ART UNIT	PAPER NUMBER
			2185	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/707,941	Applicant(s) MORI ET AL.	
	Examiner Yaima Campos	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5 and 7-10 is/are rejected.
- 7) ☒ Claim(s) 2 and 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 1/27/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The instant application having Application No. 10/707,941 has a total of 10 claims pending in the application; there are 2 independent claims and 8 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. OBJECTIONS TO THE SPECIFICATION

Claim Objections

4. **Claims 1-2 and 6-7** are objected to because of the following informalities:
5. Claim 1 recites the limitation "said has value" in line 9. It is believed that this limitation contains a typographical error and should be – **said hash value** --.
6. Claim 1 recites the limitation "comprises a first and hash function" in line 22. It is believed that this limitation contains a grammatical error and should be – **comprises a first and second hash functions** --.

7. Claim 1 recites the limitation “comprises a first and second pointer table” in line 23. It is believed that this limitation contains a grammatical error and should be – **comprises a first and second pointer tables --**.

8. Claim 2 recites the limitation “said registration means and said retrieval means uses” in lines 2-3. It is believed that this limitation contains a grammatical error and should be – **said registration means and said retrieval means use --**.

9. Claim 6 recites the limitation “registered firs item” in line 3. It is believed that this limitation contains a typographical error and should be – **registered first item --**.

10. Claim 7 recites the limitation “wherein the said registered” in line 2. It is believed that this limitation contains a typographical error and should either be – **wherein the registered – or – wherein said registered--**.

11. Claim 7 recites the limitation “data chare a pointer” in line 3. It is believed that this limitation contains a typographical error and should either be – **share --**.

12. Appropriate correction is required.

Specification Objections

13. The specification is objected to because of the following minor informalities:

14. The specification recites the limitation “a method that register data” in paragraph 0001. It is believed that this limitation contains a grammatical error and should be – **a method that registers data --**.

15. The specification recites the limitation “rooter” in paragraph 0005. It is believed that this limitation contains a typographical error and should be – **router --**.

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16. The specification recites the limitation "ProblemsFor" in paragraph 0008. It is believed that this limitation contains a typographical error and should be – **Problems. For --**

17. Applicant's cooperation is requested in correcting any other minor errors of which applicant may become aware in the specification.

18. Appropriate correction is required.

IV. REJECTIONS NOT BASED ON PRIOR ART

a. DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC § 112

19. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

20. **Claims 1-9** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

21. Claim 1 recites the limitations "selected from the group" in line 11. There is insufficient antecedent basis for these limitations in the claim. The applicants might consider amending this claim to read –**selected from a group-**.

22. Any claim not specifically addressed above, is being rejected as encompassing the deficiencies of a claim upon which it depends.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

24. **Claim 10** is rejected under 35 U.S.C. 102(e) as being anticipated by Hariguchi et al. (US 6,665,297).

25. As per **claim 10**, Hariguchi discloses “A data structure comprising: a data table where first item data are registered, each first item data having a corresponding second item data;” as **“routing packets in a network such as the Internet, and particularly to a network routing table that ensures that a destination address of a packet is mapped to a route in a fixed amount of time”** (Column 1, lines 3-6). Hariguchi further discloses searching **“for a match to a destination address”** (Column 4, line 66) wherein **“the output pointer in the pointer register 92 is used to address the route entry table 98 to select an entry 182”** (Figure 5 and **Column 8, lines 21-23**) **“a first pointer table where pointers to a first part of the registered data in said data table are registered in storage positions that are designated by hash values obtained by applying a first hash function to the first item data; and a second pointer table where pointers to a second part of the registered data in said data table are registered in storage positions that are designated by hash values obtained by applying a second hash function to the first item data of**

the other registered data;” [Hariguchi discloses this concept as “routing table 40 uses a combination of hash-based routing tables 70, a content addressable memory (CAM) based routing table 80, and pipeline architecture to consistently search for a match to a destination address” (Figure 2 and Column 4, lines 63-66). Hariguchi further discloses this limitation as “each hash circuit hashes a portion of the message destination address to provide a hashed-message-destination address. Each has circuit has a hash bucket storing output pointers at associated hash bucket addresses in the hash bucket. Each hash circuit outputs an output pointer, if any, associated with the hashed-message-destination address” (Column 3, lines 47-53)] “and a selection table where selection data representing which of said first and second pointer tables is used for searching through the registered data in said data table [Hariguchi discloses this concept as “selection circuit is connected in series with the CAM and the hash circuits. The selection circuit selects one of the output pointers output by the hash circuits and the CAM” (Column 3, lines 53-56)].

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

27. **Claims 1, 3-5 and 7-9** are rejected under 35 U.S.C. 103(a) as being anticipated by Hariguchi et al. (US 6,665,297) in view of Schnell (US 5,757,795).

28. As per **claim 1**, Hariguchi discloses “An information processing device” as [**“routing packets in a network such as the Internet, and particularly to a network routing table that ensures that a destination address of a packet is mapped to a route in a fixed amount of time” (Column 1, lines 3-6)**] “comprising: a data table having at least one first item data, each of the at least one first item data having a corresponding second item data, each of the at least one first and second item data registered;” [**With respect to this limitation, Hariguchi discloses searching “for a match to a destination address” (Column 4, line 66) wherein “the output pointer in the pointer register 92 is used to address the route entry table 98 to select an entry 182” (Figure 5 and Column 8, lines 21-23)**] “a pointer table having pointers to the registered data in said data table, said pointers referenced in storage positions, said storage positions designated by hash values, said hash values obtained by applying a predetermined hash function to the at least one first item data;” [**Hariguchi discloses this concept as “routing table 40 uses a combination of hash-based routing tables 70, a content addressable memory (CAM) based routing table 80, and pipeline architecture to consistently search for a match to a destination address” (Figure 2 and Column 4, lines 63-66)**] “and a member selected from the group consisting of registration means and retrieval means, said means comprising a means for implementing a registration for said at least one first item data and corresponding second item data in said data table and said retrieval means comprising a means for implementing a retrieval of said second item data from said data table when said first item data is retrieved,” [**With respect to this limitation, Hariguchi discloses searching “for a match to a destination address” (Column 4, line 66) as retrieval means and also discloses that during operation “the routing table is updated. New route entries are added to the hash buckets and to the**

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CAM” as registration means (Column 8, lines 60-62)] “wherein said hash function comprises a first and a second hash function and said pointer table comprises a first and second pointer table accessed using hash values derived from said corresponding first and second hash functions” [Hariguchi discloses this limitation as “each hash circuit hashes a portion of the message destination address to provide a hashed-message-destination address. Each has circuit has a hash bucket storing output pointers at associated hash bucket addresses in the hash bucket. Each hash circuit outputs an output pointer, if any, associated with the hashed-message-destination address” (Column 3, lines 47-53)].

Hariguchi does not disclose expressly that “said registration means and said retrieval means capable of being disabled by a synonym.”

Schnell discloses “registration means and said retrieval means capable of being disabled by a synonym” as [“**a method and apparatus for hashing binary or media access control addresses” in a network, (Column 1, lines 13-15) wherein “the hash logic of each of the network ports includes an address enable register for storing the bit enable” (Column 3, lines 37-40) which is used “to optimize uniqueness of correspondingly updated binary hash values” (Column 3, lines 22-24). Schnell further explains that “the enable pattern is modified to optimize hash addresses in the event the default enable pattern results in a significant amount of hash address collisions” (Column 8, lines 64-67)] as teaching the concept of enabling/disabling registrations/retrievals of addresses in a hash table.**

Hariguchi (US 6,665,297) and Schnell (US 5,757,795) are analogous art because they are form the same field of endeavor of hashing control addresses in a network.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the system/method for routing packets in a network as described by Hariguchi and further include means of enabling/disabling registration/retrieval means when a significant amount of hash address collisions occur as taught by Schnell.

The motivation for doing so would have been because Schnell teaches that means of enabling/disabling registration/retrieval means when a significant amount of hash address collisions occur [**“provides an improved apparatus and method for sorting and tracking addresses in a networking environment” (Column 4, lines 28-29) as it assists “to optimize uniqueness of correspondingly updated binary hash values” (Column 3, lines 22-24)**].

Therefore, it would have been obvious to combine Hariguchi et al. (US 6,665,297) and Schnell (US 5,757,795) for the benefit of creating a hashing method/system for address control in a network to obtain the invention as specified in claim 1.

29. **Claim 1** further requires:

“a means for implementing a registration” (paragraph 0008 of applicant’s specification identifies this means as “registration means 102” and further explains having “a hardware structure for executing a program according to the present invention” (Figure 2). Applicant further describes “MAC address table 3” as registration means in paragraph 0029)

[Hariguchi discloses this limitation as “addition of new route entry to the hash bucket 160 of the routing table” and explains having a “CPU_addr” identifying a destination and “Search/CPU” command line used to initial a registration process (Column 8, lines 60-65)]

“a means for implementing a retrieval” (paragraph 0008 of applicant’s specification identifies this means as retrieval means 102 and further explains having “a hardware structure for

executing a program according to the present invention” (Figure 2). Applicant further describes “MAC address table 3” as retrieval means in paragraph 0047) [Hariguchi discloses this limitation as “in a search, the routing table 40 simultaneously searches the hash-based routing tables 80 and the CAM-based routing table 80 for the destination address, then outputs an output pointer associated with the longest match to the destination address” (Columns 4-5, lines 67 and 1-5)].

30. As per claim 3, the combination of Hariguchi and Schnell discloses “An information processing device according to claim 1,” [See rejection to claim 1 above] “wherein each of the registered data in said data table is designated by a pointer that is accessed by at most one of said first and second pointer tables” [Hariguchi discloses this concept as “the route entry table stores a complete set of information needed to route a datagram and thereby allows the hash circuits and, in an alternate embodiments, the CAM, to store pointers” (Column 5, lines 39-41)].

31. As per claim 4, the combination of Hariguchi and Schnell discloses “An information processing device according to claim 1,” [See rejection to claim 1 above] “further comprising a selection table having selection data, said selection data identifying which of said first hash function and said first pointer table and said second hash function and said second pointer table are selected, said selection table used when searching through the respective registered data in said data table” [With respect to this limitation, Hariguchi discloses that a “selection circuit is connected in series with the CAM and the hash circuits. The selection circuit selects one of the output pointers output by the hash circuits and the CAM” (Column 3, lines 53-56)].

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32. As per claim 5, the combination of Hariguchi and Schnell discloses “An information processing device according to claim 1,” [See rejection to claim 1 above] “wherein said registration means implements the registration of said first item data into said data table using said first pointer table, said registration means verifying that said first item data is not registered in first pointer table or the second pointer table” [Hiraguchi discloses this concept as when “the addition of a new route entry to the hash bucket of the routing table” is to be done, “a destination address is supplied by the microprocessor” and “is input to the mask circuit;” then “the hash function generator circuit generates a hash value based on the supplied address.” Wherein “the data mask circuit acts as a driver when writing data to the hash bucket. If the entry to the hash bucket at the generated hash value is empty, the supplied output pointer is stored in that address,” which comprises a situation when no synonyms are found as the “hit/miss signal from the hash bucket indicates a miss” (Columns 8-9, lines 60-67 and 1-11)].

33. As per claim 7, the combination of Hariguchi and Schnell discloses “An information processing device according to claim 1,” [See rejection to claim 1 above]. Hariguchi discloses that “said first item data share a pointer in said first registered first item data table and said pointer table, said registration means causing all additional synonymous registrations to be registrations in the second pointer table” as [With respect to this limitation, Hariguchi discloses that “when the entry to the hash bucket already stores another route entry, as when the hit/miss signal indicates a hit, the destination address” is “stored in the CAM 80. When the CAM already has an entry for a destination address, the prefix length and output pointer are updated for that destination address”(Column 9, lines 12-17)] but fails to

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disclose expressly that “said registration means allowing a predetermined number of synonymous registrations.”

Schnell discloses that “said registration means allowing a predetermined number of synonymous registrations” as [**“a method and apparatus for hashing binary or media access control addresses” in a network, (Column 1, lines 13-15) wherein “a certain amount of processing for handling address collisions is tolerated until reaching the threshold” (Column 12, lines 60-61), and further explains that “the threshold is determined statistically” and “may be any acceptable value depending upon the particular embodiment and configuration” Columns 12-13, lines 64-67 and 1-2].**

Hariguchi (US 6,665,297) and Schnell (US 5,757,795) are analogous art because they are form the same field of endeavor of hashing control addresses in a network.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the system/method for routing packets in a network as described by Hariguchi and further include means of allowing a predetermined number of collisions (threshold) to occur in a hashing table before starting address registrations into a second hashing table or allowing any other processing to occur as taught by Schnell .

The motivation for doing so would have been because Schnell teaches that means of means of allowing a predetermined number of collisions (threshold) to occur in a hashing table before taking any other processing action [**“provides an improved apparatus and method for sorting and tracking addresses in a networking environment” (Column 4, lines 28-29) since the system would save processing time as “valuable processing time is being used to handle address collisions” (Column 12, lines 63-64)].**

Therefore, it would have been obvious to combine Hariguchi et al. (US 6,665,297) and Schnell (US 5,757,795) for the benefit of creating a hashing method/system for address control in a network to obtain the invention as specified in claim 7.

34. As per **claim 8**, the combination of Hariguchi and Schnell discloses “An information processing device according to claim 1,” [See rejection to claim 1 above] “wherein said registration of said first item data and corresponding second item data includes a sender address in a packet or frame received and corresponding port identification data, and said retrieval of said first item data and corresponding second item data includes a destination address of said packet or frame and corresponding port identification data” [With respect to this limitation, Hariguchi discloses that “information is transferred through the network from a source computer to a destination computer using packets called datagrams” (Column 1, lines 9-11), that “the routers have input ports for receiving incoming datagrams and output ports for transmitting outgoing datagrams” (Column 1, lines 17-19) and further explains that “the information in a route entry in a routing table includes” a “destination IP address,” and “address port information” (Column 1, lines 39-41)].

35. As per **claim 9**, the combination of Hariguchi and Schnell discloses “An information processing device according to claim 8,” [See rejection to claim 8 above] “wherein said sender and destination addresses are MAC addresses, and the device functions as a switch device that transfers the received packet or frame from a corresponding port to the destination MAC address in said received packet or frame” [With respect to this limitation, Schnell discloses[“a method and apparatus for hashing binary or media access control addresses” in a network, (Column 1, lines 13-15) in which “a network switch for transferring data packets according

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to the present invention includes a plurality of network ports” (Column 2, lines 63-64) and further discloses that “the binary address values are media access control (MAC) addresses used for uniquely identifying network devices” (Column 3, lines 29-31)].

VI. RELEVANT ART CITED BY THE EXAMINER

36. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant’s art and those arts considered reasonably pertinent to applicant’s disclosure. See **MPEP 707.05(c)**.

37. The following references teach hashing control addresses in a network.

U.S. PATENT NUMBER

US 6,212,525

US 6,862,602

US 5,920,900

US 6,697,873

US 6,434,662

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

38. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) SUBJECT MATTER CONSIDERED ALLOWABLE

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39. Per the instant office action, claims 2 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reasons for allowance of claims 2 and 6 in the instant application is the combination with the inclusion in these claims of the limitation of an information system wherein **“wherein said registration means and said retrieval means uses said first hash function and said first pointer table when enabled and said second hash function and said second pointer table when disabled.”** The prior art of record including the disclosures under section **VI** above neither anticipates nor renders obvious the above recited combination.

a(2) CLAIMS REJECTED IN THE APPLICATION

40. Per the instant office action, claims 1, 3-5 and 7-10 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

42. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained

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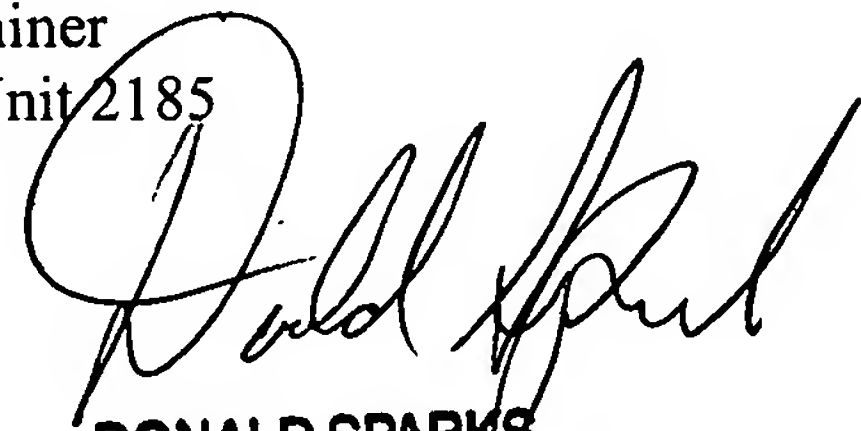
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January 23, 2006

Yaima Campos

Examiner

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A handwritten signature in black ink, appearing to read "Donald Sparks", written over a circular stamp.

DONALD SPARKS
SUPERVISORY PATENT EXAMINER